

Amendments to the Claims:

Please cancel claim 5, and amend claims 1 and 6 as shown in the following listing of claims. This listing of claims will replace all prior versions, and listings, of claims in the application.

- 1 1. (currently amended) A driver circuit comprising:
2 an output transistor connected between a voltage terminal and an
3 output node to produce an output signal on said output node, said output transistor
4 including a control terminal;
5 a current source connected to said control terminal of said output
6 transistor to provide a reference current, said current source being configured to
7 generate said reference current proportional to a reference voltage and a reference
8 frequency; and
9 a feedback capacitor connected from said output node to said
10 control terminal of said output transistor to control said output transistor as a
11 function of a difference between current through said capacitor and said reference
12 current.
- 1 2. (original) The driver circuit of claim 1 further comprising a memory
2 operatively connected to said control terminal of said output transistor, said
3 memory being configured to store a signal on said control terminal of said output
4 transistor from a previous operating cycle in which said output transistor was
5 activated.
- 1 3. (original) The driver circuit of claim 2 wherein said memory includes a
2 memory capacitor and an amplifier, said amplifier being connected to said
3 memory capacitor and said output transistor such that said amplifier is selectively
4 configured in a voltage follower configuration to store said signal on said control
5 terminal of said output transistor in said memory capacitor.

1 4. (original) The driver circuit of claim 3 further comprising a controlled
2 switch located between said memory capacitor of said memory and said control
3 terminal of said output transistor, said switch comprising a control input
4 connected to said output node.

1 5. (canceled).

1 6. (currently amended) The driver circuit of claim 1 wherein said current
2 source includes a frequency-to-current converter.

1 7. (original) The driver circuit of claim 1 further comprising a first switch
2 located between said voltage terminal and said output transistor and a second
3 switch located between said current source and said control terminal of said output
4 transistor, said first and second switches being controlled by an input signal.

1 8. (original) The driver circuit of claim 1 further comprising:
2 a second output transistor connected between said output node and
3 a second voltage terminal, said second output transistor including a control
4 terminal;
5 a second current source connected to said control terminal of said
6 second output transistor; and
7 a second feedback capacitor connected from said output node to
8 said control terminal of said second output transistor.

1 9. (original) A driver circuit comprising:
2 an output transistor connected between a voltage terminal and an
3 output node to produce an output signal on the output node, said output transistor
4 including a control terminal;
5 a memory connected to said control terminal of said output
6 transistor, said memory being configured to store a signal on said control terminal
7 from a previous operating cycle in which said output transistor was activated;
8 a current source connected to said control terminal of said output
9 transistor to provide a reference current; and
10 a feedback capacitor connected from said output node to said
11 control terminal of said output transistor to control a rate of signal change on said
12 output node.

1 10. (original) The driver circuit of claim 9 wherein said memory includes a
2 memory capacitor and an amplifier, said amplifier being connected to said
3 memory capacitor and said output transistor such that said amplifier is selectively
4 configured in a voltage follower configuration to store said signal on said control
5 terminal of said output transistor in said memory capacitor.

1 11. (original) The driver circuit of claim 10 further comprising a controlled
2 switch located between said memory capacitor of said memory and said control
3 terminal of said output transistor, said switch comprising a control input
4 connected to said output node.

1 12. (original) The driver circuit of claim 9 wherein said current source is
2 configured to generate said reference current proportional to a reference voltage
3 and a reference frequency.

1 13. (original) The driver circuit of claim 12 wherein said current source
2 includes a frequency-to-current converter.

1 14. (original) The driver circuit of claim 12 further comprising a first switch
2 located between said voltage terminal and said output transistor and a second
3 switch located between said current source and said control terminal of said output
4 transistor, said first and second switches being controlled by an input signal.

1 15. (original) The driver circuit of claim 9 further comprising:
2 a second output transistor connected between said output node and
3 a second voltage terminal, said second output transistor including a control
4 terminal;
5 a second memory connected to said control terminal of said second
6 output transistor, said second memory being configured to store a signal on said
7 control terminal of said second output transistor from a previous operating cycle
8 when said second output transistor was activated;
9 a second current source connected to said control terminal of said
10 second output transistor to provide a second reference current; and
11 a second feedback capacitor connected from said output node to
12 said control terminal of said second output to control a second rate of signal
13 change on said output node.

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1 16. (original) A method for driving an electrical device, said method
2 comprising:
3 receiving an input signal;
4 applying a stored signal to an output transistor in response to said
5 input signal to produce an output signal on an output node; and
6 controlling said output signal on said output node using a
7 difference between a reference current and current capacitively fed back from said
8 output node.

1 17. (original) The method of claim 16 further comprising storing a control
2 signal on said output transistor as said stored signal.

1 18. (original) The method of claim 16 wherein said controlling includes
2 generating said reference current using a reference frequency and a reference
3 voltage, and applying said reference current to a control terminal of said output
4 transistor.

1 19. (original) The method of claim 16 further comprising:
2 applying a second stored signal to a second output transistor in response to said
3 input signal to change said output signal on said output node; and
4 controlling said output signal on said output node using a difference between a
5 second reference current and current through a second capacitive feedback from
6 said output node to said second output transistor.

1 20. (original) The method of claim 19 further comprising alternately activating
2 said output transistor and said second output transistor.